AMENDMENTS TO THE CLAIMS

Please amend claims 1-6 as follows:

1. (currently amended) A method of manufacturing a semiconductor device, comprising ~~the steps of~~:

~~forming a first well region by~~ performing ~~an~~ a first ion implantation process for implanting first ions into a first region of a semiconductor substrate; ~~,and then forming a second well region in the first well region by~~

performing ~~an~~ a second ion implantation process for implanting second ions into the first region wherein the second ions having a larger mass than the first ions; and

~~forming a well region by~~ performing an annealing process on the ~~result~~ resulting structure to form a three-fold well region having a first lower well region implanted with the first ions, a second middle well region implanted with the second ions and a third upper well region implanted with the first ions.

2. (currently amended) A method of claim 1, wherein the ~~first well region is formed~~ first ion implantation process is performed by implanting phosphorus (P) ions at a tilt angle in the range of 3° to 13° with a dose in the range of 1E11 ions/cm^2 to 1E14 ions/cm^2 at an energy in the range of about 500 KeV to 3000KeV, by using a high-energy ion implantation device.

3. (currently amended) A method of claim 1, wherein the second ~~well region is formed~~ ion implantation process is performed by implanting arsenic (As) ions having larger mass than phosphorus ions, at a tilt angle in the range of 3° to 13° with a dose in the range of 1E11 ions/cm^2 to 1E14 ions/cm^2 at an energy in the range of about 100 KeV to 300KeV, by using a middle-current ion implantation device.

4. (currently amended) A method of claim 1, wherein the annealing process is performed using one of an RTP process performed under N_2 or H_2 gas atmosphere at a temperature in the range of 900°C to 1000°C for ~~10seconds~~ a time period in the range of 10 minutes to 60 seconds, or a furnace process performed under N_2 or H_2 gas atmosphere at a temperature in the range of 900°C to 1100°C for ~~10minutes~~ a time period in the range of 10 minutes to 60 minutes.

5. (currently amended) A method of claim 1, further comprising ~~the steps of~~ forming a region into which ions for adjusting a threshold voltage are implanted on the semiconductor substrate on which well regions are formed, and then forming a tunnel oxide film, a floating gate electrode, a dielectric film and a control gate electrode on an upper part of the semiconductor substrate.

6. (currently amended) A method of claim 1, further comprising ~~a step of~~ forming a screen oxide film serving as a buffer layer for suppressing a damage generated by the ion implantation process for forming the first well region and the second well region before forming the well region.